AMENDMENTS TO CLAIMS

1 (original). Driver (150) for a gas discharge lamp (9), comprising:

two input terminals (51a, 52b) for connection to a source of substantially DC voltage;

two output terminals (52a, 52b) for connection to a gas discharge lamp (9);

an arrangement of two controllable switches (61, 62) connected in series between said two input terminals (51a, 52b);

an inductor (73) connected in series with said two output terminals (52a, 52b), this series arrangement being coupled to a node (P) between said two switches (61, 62);

a control unit (180) having two control outputs (81, 82) coupled to provide control signals (S1, S2) to said two controllable switches (61, 62);

the control unit (180) being designed to generate its control signals (S1, S2) at relatively low-frequency commutation intervals (41, 42) and in relatively high-frequency operational phases (43, 44), such that during a first commutation interval (41) a lamp circuit current (I_{LC}) has substantially only a first direction, while during a second commutation interval (42) the lamp circuit current (I_{LC}) has substantially only a second direction opposite to the first direction, and such that during a first operational phase (43) the lamp circuit current (I_{LC}) has a substantially continuously increasing level, while during a second operational phase (44) the lamp circuit current (I_{LC}) has a substantially continuously decreasing level;

wherein the control unit (180) is designed to generate its control signals (S1, S2) such that said two switches (61, 62) are always switched substantially simultaneously in counter-phase.

2 (original). Driver according to claim 1, wherein the control unit (180) is designed to generate its control signals (S1, S2) such that:

- during the first commutation interval (41) and the first operational phase (43), a first switch (61) coupled between said node (P) and a positive input terminal (51a) is substantially conductive, while a second switch (62) coupled between said node (P) and a negative input terminal (51b) is substantially non-conductive;

- during the first commutation interval (41) and the second operational phase (44), said first switch (61) is substantially non-conductive while said second switch (62) is substantially conductive;
- during the second commutation interval (421) and the first operational phase (43), said first switch (61) is substantially non-conductive while said second switch (62) is substantially conductive;
- during the second commutation interval (42) and the second operational phase (44), said first switch (61) is substantially conductive while said second switch (62) is substantially non-conductive.

3 (currently amended). Driver according to claim 1 [[~~or 2~~]], wherein said switches (61, 62) comprise MOSFET switches.

4 (currently amended). Driver according to claim 1 ~~any of claims 1-3~~, adapted to switch from the second operational phase (44) to the first operational phase (43) at a moment when the lamp circuit current (I_{LC}) reaches a predetermined low current level (I_{LOW}).

5 (currently amended). Driver according to claim 1 ~~any of claims 1-4~~, adapted to switch from the second operational phase (44) to the first operational phase (43) at a moment when the lamp circuit current (I_{LC}) is substantially zero.

6 (currently amended). Driver according to claim 1 ~~any of claims 1-5~~, adapted to switch from one commutation interval (41; 42) to a subsequent commutation interval (42; 41) at a moment when the lamp circuit current (I_{LC}) reaches a predetermined low current level (I_{LOW}).

7 (currently amended). Driver according to claim 1 ~~any of claims 1-6~~, adapted to switch from one commutation interval (41; 42) to a subsequent commutation interval (42; 41) at a moment when the lamp circuit current (I_{LC}) is substantially zero.

8 (currently amended). Driver according to claim 5 [[~~or 7~~]], further comprising a zero crossing detector (100) arranged to sense the lamp circuit current (I_{LC}) and to generate an output signal (S_D) indicative of the lamp circuit current (I_{LC}) crossing zero, the control unit (180) having an input (183) coupled to receive said detector output signal (S_D).

9 (original). Detector (100) for sensing a current and for generating an output signal (S_D) indicative of said current crossing zero,

the detector comprising a transformer (110) having a primary winding (111) for receiving the current to be sensed and further comprising a secondary winding (112) inductively coupled to said primary winding (111), the transformer (110) being designed such as to be magnetically saturated already at a very low current saturation level.

10 (currently amended). Detector according to claim 9, said current saturation level being in the order of about 200 mA[[,]] ~~or preferably lower~~.

11 (currently amended).Detector according to claim 9 [[~~or 10~~]], further comprising:

a first diode (113) having a first terminal (anode) coupled to a first end terminal of the secondary winding (112);

a second diode (114) having a first terminal (anode) coupled to a second end terminal of the secondary winding (112) and having its second terminal (cathode) connected to the second terminal (cathode) of the first diode (113);

a resistor (115) having one terminal connected to the node between said two diodes (113, 114) and having its other terminal coupled to a central tap of the secondary winding (112).

12 (original). Detector according to claim 11, further comprising a Zener diode (116) coupled between said resistor (115) and said central tap of the secondary winding (112).

13 (currently amended). Driver (150) for a gas discharge lamp (9), comprising:

two input terminals (51a, 52b) for connection to a source of substantially DC voltage;

two output terminals (52a, 52b) for connection to a gas discharge lamp (9);

an arrangement of two controllable switches (61, 62) connected in series between said two input terminals (51a, 52b);

an inductor (73) connected in series with said two output terminals (52a, 52b), this series arrangement being coupled to a node (P) between said two switches (61, 62);

a control unit (180) having two control outputs (81, 82) coupled to provide control signals (S1, S2) to said two controllable switches (61, 62);

the control unit (180) being designed to generate its control signals (S1, S2) at relatively low frequency commutation intervals (41, 42) and in relatively high frequency operational phases (43, 44), such that during a first commutation interval (41) a lamp circuit current (I_{LC}) has substantially only a first direction while during a second commutation interval (42) the lamp circuit current (I_{LC}) has substantially only a second direction opposite to the first direction, and such that during a first operational phase (43) the lamp circuit current (I_{LC}) has a substantially continuously increasing level while during a second operational phase (44) the lamp circuit current (I_{LC}) has a substantially continuously decreasing level;

the driver further comprising a zero crossing detector (100) according to claim 9 ~~any of claims 9-12~~, wherein said primary winding (111) is connected in series with the driver output terminals (52a, 52b), the control unit (180) having an input (183) coupled to receive said detector output signal (S_D).

14 (currently amended). Driver according to claim [[~~8 or~~]] 13, comprising:

a first flip-flop device (220) being switched at a relatively high frequency corresponding to the operational phases (43, 44);

a second flip-flop device (230) having a signal input (231) for receiving a commutation clock signal (φ_{COMM}), a trigger input (232) coupled to an output (223) of said first flip-flop device (220), and at least one output (224);

a first XNOR device (280) having a first input (281) coupled to an output (224) of said first flip-flop device (220), having a second input (282) coupled to an output

(234) of said second flip-flop device (230), and having an output (283) coupled to the first output (81) of the control unit (180).

15 (currently amended). Driver according to claim 13 ~~any of claims 8 or 13-14~~, comprising a first triggerable timer device (240) having at least one output (242) coupled to a set input (225) of said first flip-flop device (220) [[~~and/or~~]] and comprising a second triggerable timer device (250) having at least one output (252) coupled to a reset input (226) of said first flip-flop device (220).

16 (currently amended). Driver according to claim 13 ~~any of claims 8 or 13-15~~, comprising a current detector (260) having at least one output (262) coupled to a reset input (226) of said first flip-flop device (220).

17 (currently amended). Driver according to claim 13 ~~any of claims 8 or 13-16~~, further comprising:

a second XNOR device (290) having a first input (291) coupled to receive a signal (Q_{224}) logically identical to the signal received by one input (281) of said first XNOR device (280), having a second input (292) coupled to receive a signal (Q_{233}) logically opposite to the signal received by the other input (281) of said first XNOR device (280), and having an output (293) coupled to the second output (82) of the control unit (180).

18 (currently amended). Driver according to claim 14 ~~any of claims 14-17~~, wherein a signal input (221) of said first flip-flop device (220) is coupled to receive a constant HIGH signal, and wherein a trigger input (222) of said first flip-flop device (220) is coupled to said input (183) for receiving said detector output signal (S_D).

19 (currently amended). Driver according to claim 13 ~~any of claims 8 or 13-18, said zero-crossing detector (100) being designed according to any of claims 9-12~~, wherein said primary winding (111) is connected in series with the driver output terminals (52a, 52b).